An FPGA-based High Speed Parallel Signal Processing System for Adaptive Optics Testbed

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ABSTRACT

In this paper a state-of-the-art FPGA (Field Programmable Gate Array) based high speed parallel signal processing system (SPS) for adaptive optics (AO) testbed with 1 kHz wavefront error (WFE) correction frequency is reported. The AO testbed consists of Shack-Hartmann sensor (SHS) and deformable mirror (DM), tip-tilt sensor (TTS), tip-tilt mirror (TTM) and an FPGA-based high performance SPS to correct wavefront aberrations. The SHS and DM are composed of several hundreds of subapertures and actuators, respectively, with Fried geometry, requiring a high speed parallel computing capability SPS. In this study, the target WFE correction speed is 1 kHz; therefore, it requires massive parallel computing capabilities as well as strict hard real time constraints on measurements from sensors, matrix computation latency for correction algorithms, and output of control signals for actuators. In order to meet them, an FPGA based real-time SPS with parallel computing capabilities is proposed. In particular, the SPS is made up of a National Instrument's (NI's) real time computer and five FPGA boards based on state-of-the-art Xilinx Kintex 7 FPGA. Programming is done with NI's LabView environment, providing flexibility when applying different algorithms for WFE correction. It also facilitates faster programming and debugging environment as compared to conventional ones. One of the five FPGA's is assigned to measure TTS and calculate control signals for TTM, while the rest four are used to receive SHS signal, calculate slops for each subaperture and correction signal for DM. With this parallel processing capability of the SPS the overall closed-loop WFE correction speed of 1 kHz has been achieved. System requirements, architecture and implementation issues are described; furthermore, experimental results are also given.

1. INTRODUCTION

To reduce atmospheric turbulence adaptive optics (AO) technologies has been developed, which basically consists of wavefront sensors to measure wavefront error (WFE), computer system for AO algorithms and adaptive mirrors to correct WFE [1]. Recently, as resolution and speed of wavefront sensor and adaptive mirror increases a lot, high performance computational system becomes indispensable. Due to its inherent parallel processing capabilities, modern FPGA (Field Programmable Gate Array) based system has been widely used for AO systems [2]-[4]. In this study the AO testbed comprises a Shack Hartmann sensor (SHS) with several hundreds of subapertures, a deformable mirror (DM) with more than two hundred actuators, a tip-tilt sensor (TTS), a tip-tile mirror (TTM), an SPS and a system controller. Its target processing rate is 1 kHz, suggesting high performance SPS is necessary. Specifically, the amount of data output from the SHS used in this study is more than 1 Gbps and matrix computation for AO algorithms demands more than 100 mega multiply-accumulate operations. Thus, high-speed and massive parallel computing capabilities are required of the SPS. To this end National Instrument's (NI's) LabView based commercial boards including FPGAs have been adopted and implemented for the SPS. The SPS has been integrated in the AO testbed and several experiments have been carried out to show that it achieves successfully the challenging requirements

The AO system considered in this study is conceptually described in Fig. 1, where the light from a star is distorted by atmospheric turbulence, goes through the telescope and is reflected by a tip-tilt mirror and a deformable mirror, sequentially. In order to measure and observe the light departing from the DM, it is divided into three paths: observation camera, tip-tilt sensor, and wavefront sensor. A SHS is used to measure WFE and a DM to correct it. The main function of SPS is threefold: (1) to gather measuring data from SHS and TTS, (2) run AO algorithms to

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calculate commands to control the DM and TTM, and (3) output the commands appropriately formatted for the DM and TTM. Note that there are two control paths. The first path goes from SHS through SPS to DM for high-order WFE correction, while the second runs from TTS through SPS to TTM to correct overall tip-tilt error. Both SHS and TTS are synchronized for proper operations. Target time latency for each path is less than or equal to 1 ms. This is a challenging objective considering complicated interface requirements of the sensors and controller and WFE correction algorithms which normally include large scale matrix calculations. A solution to this problem is to carefully divide it into smaller ones so as to make the most use of parallel processing capabilities of FPGAs.

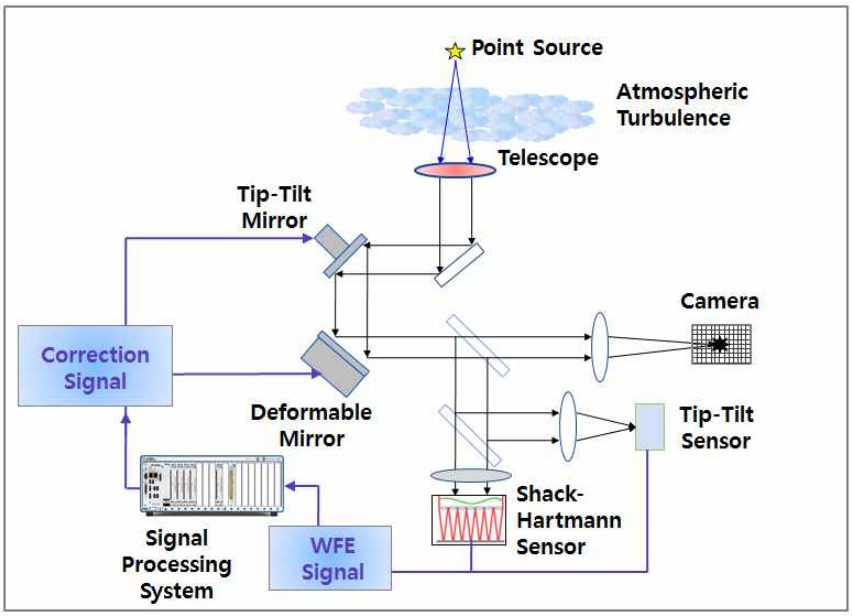


Fig. 1. Adaptive optics system for correcting atmospheric turbulence.

This paper is organized as follows. Detailed description of the SPS including design and implementation issues is given in the next section. Experimental results are described in section 3, and in section 4 concluding remarks finalize the paper.

2. Signal Processing System

The design of SPS for high speed AO system is one of the main challenging issues as processing rate becomes higher and the amount of data to be processed grows massive [2][3]. For example, in this study, target processing rate of SPS is 1 kHz and SHS output data rate is more than 1 Gbps; in addition, AO algorithm requires more than 100 mega multiply-accumulate operations. Thanks to recent advances of FPGA technologies, simple and compact H/W system can meet the requirements. When designing a SPS, one should take several factors into consideration. First, I/F complexity and latency of sensors and actuators should carefully be examined. The SHS sensor in our study has an unusual order of pixel output data as indicated in Fig. 3, which requires reordering of the frame data before further processing. This leads to unavoidable time latency in the SPS. DM is another example of which more time latency is induced as described later due to its own protocol for communication. Second, one should consider algorithmic complexity including matrix calculation cost for correcting WFE. Constant variables and matrices which do not change during operation should be prepared offline before online operation. Large scale matrix multiplication is easily implemented with modern FPGA technologies. Furthermore, graphic programming environment of LabView facilitates FPGA programming and debugging which is quite different from conventional FPGA programming process. As for correction algorithms, zonal and modal algorithms are implemented [5]~[7], which should be well optimized in terms of time latency. In our case, more than 100 mega multiply-accumulate operations are necessary for the correction algorithms which run with a period of 1 ms.

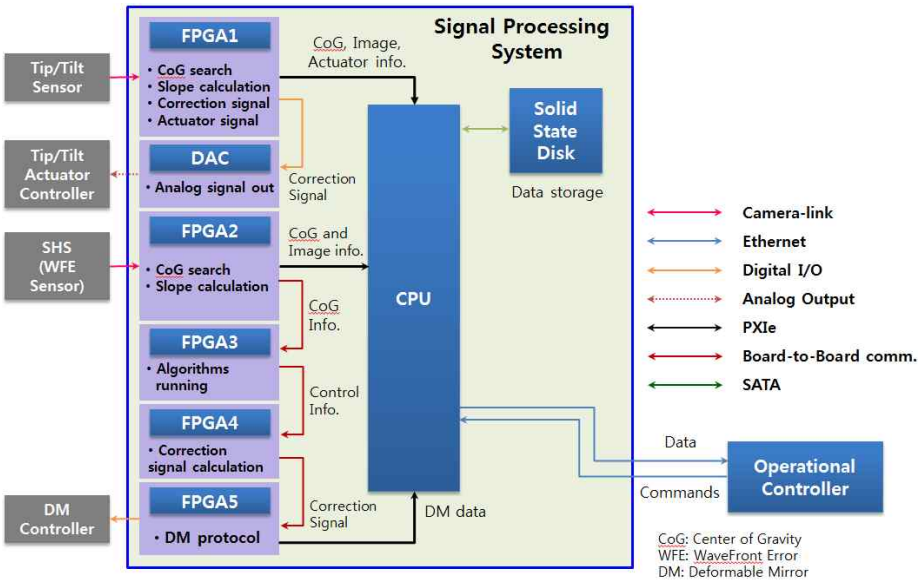


Fig. 2. Signal flow of the proposed SPS

After having taken into account the I/F complexity of sensors, controllers and computational cost of the WFE correction algorithms, we have designed a SPS based on NI's commercial boards including five FPGA ones as shown in Fig. 2. The SPS has the following hardware:

- Five identical FPGA boards, each with one Xilinx's Kintex 7 FPGA
- One CPU board with Intel i7 core
- Digital to Analog converter board for TTM controller
- Camera-link I/F adaptors for reading TTS and SHS data
- Digital I/O board for DM controller
- NI's 18-Slot 3U PXI express chassis (Fig. 4)

Due to strict real-time constraints for correcting TT error and WFE three main functions of SPS is fulfilled in FPGA boards, resulting in constant time consumption without jitter. For TT error correction, one FPGA board (FPGA #1) is enough because its computation involved is simple. It receives TTS data through Camera-link adaptor, finds center of gravity (CoG) of the image, calculates slope, runs correction algorithm, and outputs correction signal to the TTM actuator through digital to analog converter.

On the other hand, for high-order aberration four FPGA boards (FPGA #2~5) are necessary to fulfill the function. This is mainly because it includes high order matrix multiplications, complicated and time-consuming I/F of SHS and DM controller. The SHS used in our system has hundreds of subapertures, each with 12x12 pixels.
Note that although PXIe bus is available for exchanging data between boards, direct board-to-board communication line is utilized between FPGA boards to reduce time latency. Eight board-to-board direct communication lines are available in the chassis. FPGA #2 board receives SHS output data through CameraLink adaptor and calculates CoG and slope for each subaperture. Due to complicated data output sequence of SHS used in this study, reconstruction operation for each frame should be done for next processing. Fig. 3 shows the order by which the pixels are sent by the camera. Eight channel data comes from the SHS simultaneously, and each pixel has 14 bit unsigned integer values. With two bits padding, one pixel format consists of 16 bits wide data. 64 bit packet composed of four pixel data comes from the SHS at a time. The total amount of data from the SHS is more than 1 Gbps.

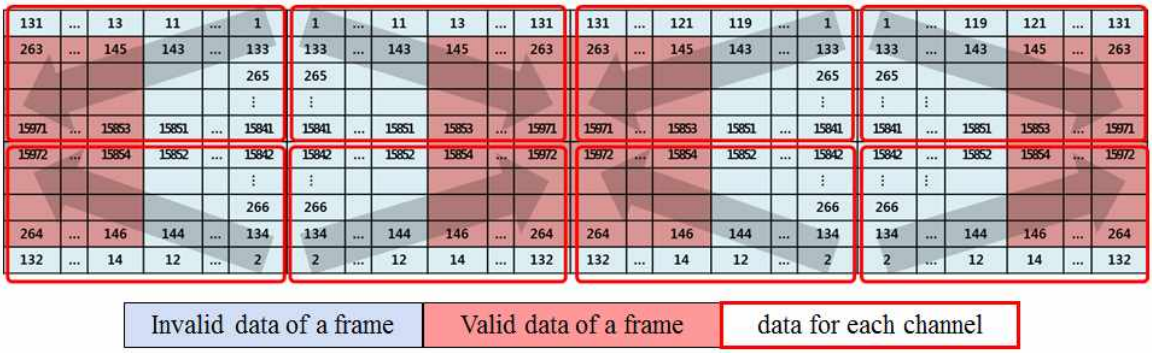
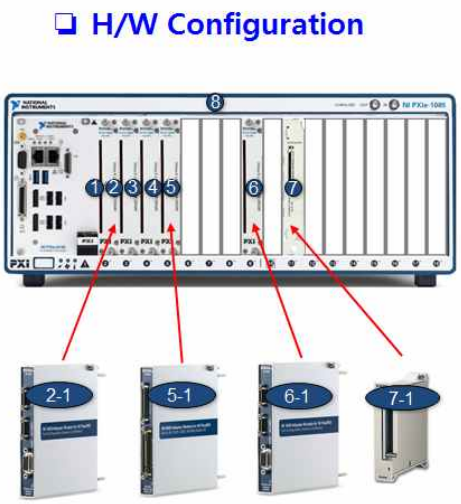


Fig. 3. Shack-Hartmann sensor data output sequence.

In FPGA #3 board, part of WFE correction algorithms are running; in particular, CoG calculation for each subaperture is accomplished. Concerning WFE correction algorithm, two algorithms, zonal and modal, have been implemented and experimented in this study. Detailed description of them is beyond the scope of the paper. Refer to the references [5]-[7] for further information. However, it would be worthwhile here to mention the time latency of 176 μs for zonal algorithm thanks to parallel computation capability of FPGA boards. Matrix calculation is carried out on FPGA #4 board, and its results are sent to FPGA #5 board where they are formatted and sequenced so as to be appropriate for the DM controller. Some of the results of each FPGA board are periodically transferred to the CPU board for analysis.

The H/W configuration of SPS is shown in Fig. 4, which is composed of 18-slot PXIe chassis, CPU board with NI's real-time OS, adaptors for sensor I/F, FPGA boards, and analog output boards.



	Function
1	• CPU with RT OS
2-1	• CameraLink input adaptor for SHS
2	• Higher order WFE processing board
3	• DM controller calculation for each subaperture
4	• Correction signal calculation
5	• Processing for DM protection and protocol
5-1	• VHDCI output adaptor
6-1	• CameraLink input adaptor for TTS
6	• TTS processing board
7	• TTM controller board
7-1	• Analog output adaptor
8	• Chassis

Fig. 4. H/W configuration of the SPS

NI's LabView environment provides graphical programming environment in contrast to conventional text-based programming environment. Moreover, unlike conventional HDL (Hardware Description Language) which is necessary for FPGA design, LabView also provides graphical programming environment for FPGA. This facilitates programming with reduced verification efforts at the cost of some overhead. Part of FPGA LabView programming for SHS I/F is shown in Fig. 5 as an example.

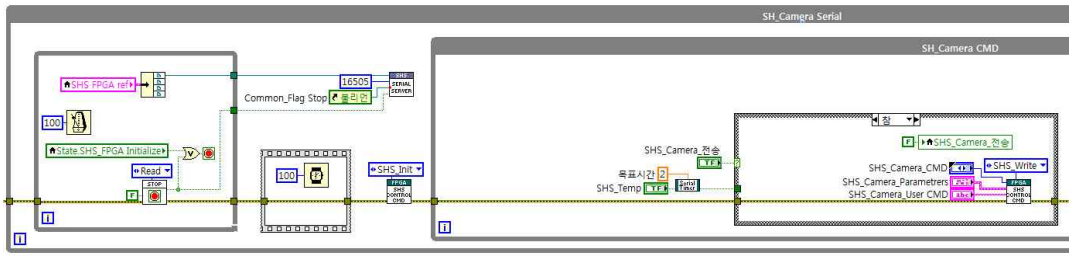


Fig. 5. LabView programming example

An SPS graphic user interface (GUI) has been developed as shown in Fig. 6. It operates in MS windows on PC, which connects to SPS through gigabit Ethernet to interchange information. The GUI comprises all the necessary interfaces for control, monitor and data logging. For instance, they include functions such as initial value setting, built-in-test for SPS and sensors, correction algorithm parameter setting, system running and stopping, subaperture selection, actuator status and image display, system performance display and so on.

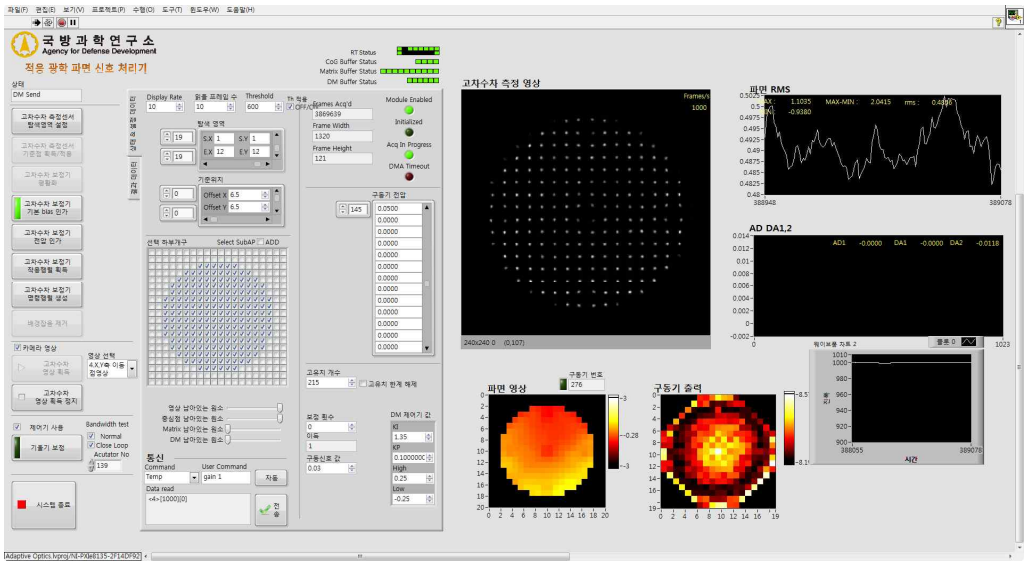


Fig. 6. Graphic user interface of the SPS

3. EXPERIMENTAL RESULTS

The SPS developed in this study has been experimented together with AO testbed. Fig. 7 indicates time latency in SHS spent by sensor data reading, algorithm calculations and control command output to DM. Specifically, SHS data reading consumes 603 μs, algorithm running (CoG calculation, matrix calculations, DM commands preparation) spends 97 μs, and DM commands output latency is 38 μs, resulting in a total time latency of 738 μs. This is sufficient for the system to operate at 1 kHz rate. Similarly, signal processing latency for TTS/TTM is about 814 μs, which also includes TTS data reading, algorithm calculation and control command output to TTM. This is also fast enough for 1kHz operation.

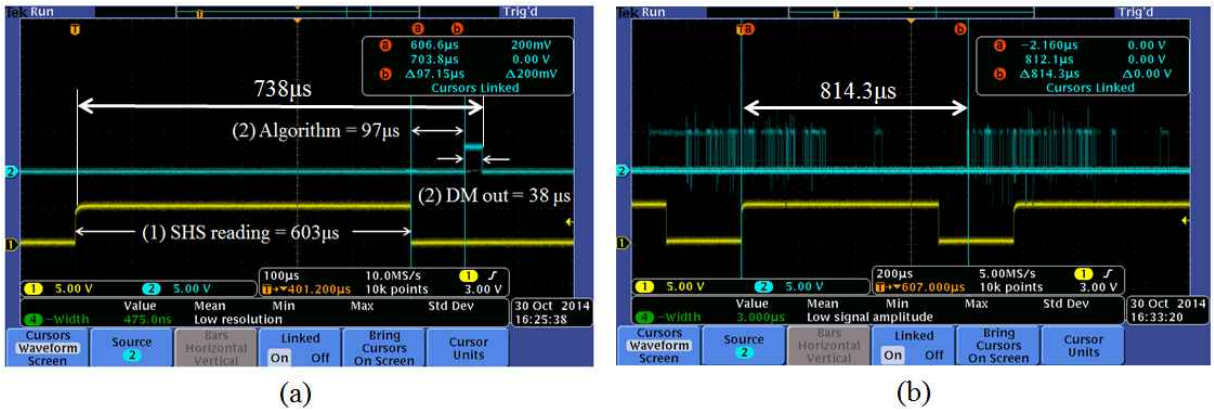


Fig. 7. Processing latency for (a) SHS→SPS→DM path and (b) TTS→SPS→TTM path.

4. CONCLUDING REMARKS

This paper has reported an FPGA based high speed parallel SPS for AO system. Target operation rate is 1 kHz, which is quite challenging for SPS design since data transfer rate and algorithmic computational complexities are high. In our system the amount of data transferred from the SHS is more than 1 Gbps and AO algorithms require more than 100 mega multiply-accumulate operations, implying high speed parallel architecture SPS is indispensable. An SPS has been designed and implemented to meet the requirements based on NI's commercial boards including FPGAs and LabView development environment. For SHS-SPS-DM path operation four NI's Xilinx Kintex 7 based FPGA boards are included, while for TTS-SPS-TTM path operation one FPGA board is involved. The SPS has been implemented in the LabView GUI programming environment, which facilitates fast development and debugging.

Experimental results have shown that time latencies are 738 µs and 814 µs, for SHS-SPS-DM and TTS-SPS-TTM paths, respectively, satisfying the target operation rate of 1 kHz. Through several successful AO experiments the SPS has proved to have enough capabilities for high performance AO systems. Note that it can be easily extended for more complicated AO systems due to its simple development environment and modern FPGA's large parallel processing capacity.

5. REFERENCES

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