SPIDER: Next Generation Chip Scale Imaging Sensor Update

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AMOS CONFERENCE PAPER

1.0 ABSTRACT

The Lockheed Martin Advanced Technology Center (LM ATC) and the University of California at Davis (UC Davis) are developing an electro-optical (EO) imaging sensor called SPIDER (Segmented Planar Imaging Detector for Electro-optical Reconnaissance) that seeks to provide a 10x to 100x size, weight, and power (SWaP) reduction alternative to the traditional bulky optical telescope and focal-plane detector array. The substantial reductions in SWaP would reduce cost and/or provide higher resolution by enabling a larger-aperture imager in a constrained volume.

Our SPIDER imager replaces the traditional optical telescope and digital focal plane detector array with a densely packed interferometer array based on emerging photonic integrated circuit (PIC) technologies that samples the object being imaged in the Fourier domain (i.e., spatial frequency domain), and then reconstructs an image. Our approach replaces the large optics and structures required by a conventional telescope with PICs that are accommodated by standard lithographic fabrication techniques (e.g., complementary metal-oxide-semiconductor (CMOS) fabrication). The standard EO payload integration and test process that involves precision alignment and test of optical components to form a diffraction limited telescope is, therefore, replaced by in-process integration and test as part of the PIC fabrication, which substantially reduces associated schedule and cost. This paper provides an overview of performance data on the second-generation PIC for SPIDER developed under the Defense Advanced Research Projects Agency (DARPA)'s SPIDER Zoom research funding. We also update the design description of the SPIDER Zoom imaging sensor and the second-generation PIC (high- and low-resolution versions).

2.0 SPIDER IMAGER DESIGN

Our SPIDER concept consists of thousands of direct-detection white-light interferometers densely packed onto PICs to measure the amplitude and phase of the visibility function at spatial frequencies that span the full synthetic aperture. The conventional approach for imaging interferometers requires complex mechanical delay lines to form the interference fringes resulting in designs that are not traceable to more than a few simultaneous spatial frequency measurements. SPIDER achieves simultaneous measurements on many baselines by employing micron-scale optical waveguides and nanophotonic structures fabricated on a PIC with micron-scale packing density to form the necessary interferometers.

The SPIDER imager samples the object visibility function in a far-field (pupil) plane (i.e., spatial frequency or uv-plane), and then digitally reconstructs an image through an inverse Fourier transform relationship. Fig. 1(a) shows an example SPIDER design consisting of lenslet arrays covered by tube assemblies to control stray light. There are 37 PIC cards beneath the lenslets. The lenslets' spacings and the radial arrangement of the PIC cards uniformly sample the object's two-dimensional Fourier transform. An alternate rectangular geometry is shown in Fig. 1(b). Fig. 1(c) illustrates that the PIC contain various components (delay lines, spectral demultiplexers, phase modulators, beam combiners, and detectors) necessary for making the visibility measurements. The largest lenslet separation (equivalent to the maximum interferometer baseline B_{max}) determines the spatial resolution of the imager. An additional circuit board contains readout and digital signal processing (DSP) electronics to process the fringe measurements and reconstruct an output image. As illustrated in Fig. 1(c), waveguides at the image plane of each lenslet collect light from different regions of the scene (the blue and red channels are waveguides and components on different PIC layers to avoid direct crossings between channels) and light collected for the same field point with different lenslets is combined to create fringes. The fringe

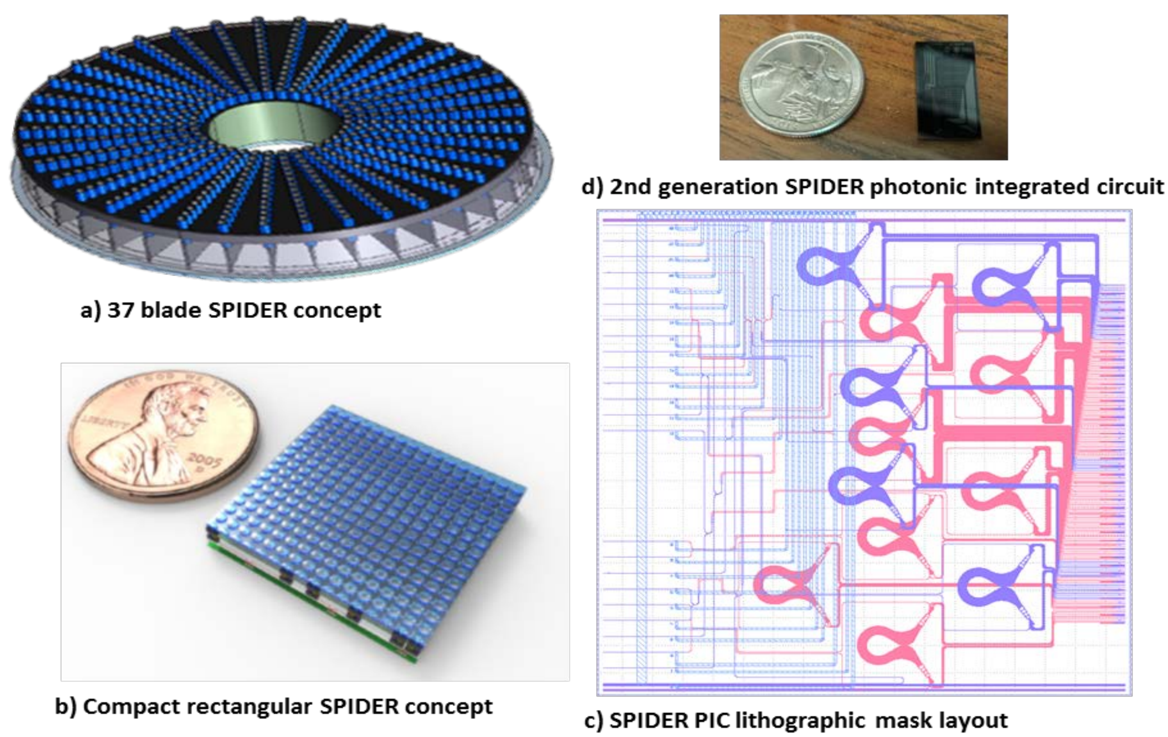


Fig. 1. (a) SPIDER azimuthal blade concept. (b) SPIDER compact rectangular array concept. (c) Schematic view of a single PIC card from the SPIDER imager. (d) Picture of the fabricated PIC.

signals are routed off of the PIC and re-imaged onto a linear detector array. In this way, the object complex visibility (amplitude and phase) are recorded for each field point and baseline, and then an image is numerically reconstructed. Fig. 1(d) shows a picture of the fabricated second-generation SPIDER PIC.

3.0 SECOND-GENERATION SPIDER ZOOM DESIGN

The second-generation SPIDER Zoom design is described in Ref 1, as presented at the 2015 AMOS conference. The interferometer baseline layout has been modified to enable a PIC design that is simpler with no waveguide crossovers. The new interferometer baseline description is shown in Fig. 2. The low-resolution PIC consists of five layers, including three layers containing waveguides. The heaters provide the ability to control the phase of the fringe and can be used to scan through a fringe temporally. There are total of 12 baselines, with the minimum baseline of 0.72 mm and maximum baseline of 20.88 mm. The arrayed waveguide grating (AWG) has 36 outputs, 2 output for 18 wavelength channels. All 12 baselines are using the exact same AWG and MMI (multi-mode interference) coupler design. The two components from the same baseline share the same AWG, one using north input and the other one using south input. Since they use the same array arms, the wavelength difference between beams is reduced to minimum.

The maximum exposure area of the photolithography tool, in this case 22 mm ×22 mm, limits the size of the SPIDER Zoom low-resolution device, which holds twelve AWGs and MMIs. The three-layer waveguide structure reduces the waveguide crossing to one crossing per channel and provides enough area to place the AWGs. The layout process is as follows: 1) put 12 AWGs in a 4×3 matrix, then assign them to each of the 150 nm waveguide layers so that AWGs from the same layer has enough spacing; 2) route each baseline channel to the closest AWG using Manhattan routing method; 3) change the layer of baselines and AWGs and add necessary layer-to-layer coupler so that overall loss from crossing and layer change is reduced to minimum; 4) add metal heaters on 1500 µm-long layer-3 waveguide, connecting the heaters to metal pads on the edge of the chip for future wire-bonding.

Note that this design is for a 1D interferometer, which is analogous to one of the PIC cards illustrated in Fig 1(a).

Low-resolution device:
Layer 1: lower 150 nm silicon nitride (Si3N4) waveguide
Layer 2: middle 50 nm Si3N4 waveguide
Layer 3: top 150 nm Si3N4 waveguide
Layer 4: heater metal layer
Layer 5: electrode metal layer

The layout of the high-resolution PIC is shown in Fig. 3, with the new low-resolution PIC design implemented. The high-resolution PIC also has five layers with layer 2 split into two parts to accommodate the additional long baseline fan-in. The design can be scaled to obtain finer resolution with a smaller field of view, by simply scaling the pupil-plane interferometer geometry. In practice, this is accomplished by adding a fan-in waveguide chip (to accommodate longer interferometer baselines) on the input side of the PIC and using larger lenslets to couple light into the PIC. Fig 3 shows the layout for a high-resolution device based on adding a fan-in chip to an existing low-resolution PIC design.

Baseline #	Baseline [mm]	NDOF	Spectral Bin #'s
1	0.72	1.0	1,18
2	1.44	2.0	1,9,18
3	2.16	2.0	2,7,12,17
4	2.88	3.0	1,5,9,13,17
5	3.60	4.0	1,4,7,10,13
6	4.32	4.0	2,5,8,11
7	5.76	6.0	2,4,6,8,10,12,14,16,18
8	7.20	7.0	1,3,5,7,9,11,13,15
9	9.36	9.0	1,3,5,7,9,11,13,15,17
10	12.24	11.0	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18
11	15.84	15.0	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18
12	20.88	19.0	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18

Spectral Bin #	Center Frequency [THz]	Spectral Width [THz]	Center Wavelength [nm]	Spectral Width [nm]
1	245	3.30	1223	16.5
2	242	3.30	1240	16.9
3	238	3.30	1257	17.4
4	235	3.30	1275	17.9
5	232	3.30	1293	18.4
6	229	3.30	1311	18.9
7	225	3.30	1331	19.5
8	222	3.30	1350	20.1
9	219	3.30	1371	20.7
10	215	3.30	1392	21.3
11	212	3.30	1413	22.0
12	209	3.30	1436	22.7
13	206	3.30	1459	23.4
14	202	3.30	1483	24.2
15	199	3.30	1507	25.0
16	196	3.30	1533	25.8
17	192	3.30	1559	26.7
18	189	3.30	1586	27.6

Fig 2. Updated description of the low-resolution PIC interferometer baselines and the spectral binning per baseline.

High-resolution device
Layer 1: lower 150 nm Si_3N_4 waveguide
Layer 2.1: middle 50 nm Si_3N_4 waveguide
Layer 2.2: contact lithography fan-in
Layer 3: top 150 nm Si_3N_4 waveguide
Layer 4: heater metal layer
Layer 5: electrode metal layer

Fabrication of the new low-resolution PIC design was completed at UC Davis; some pictures of the new devices are shown in Fig. 4.

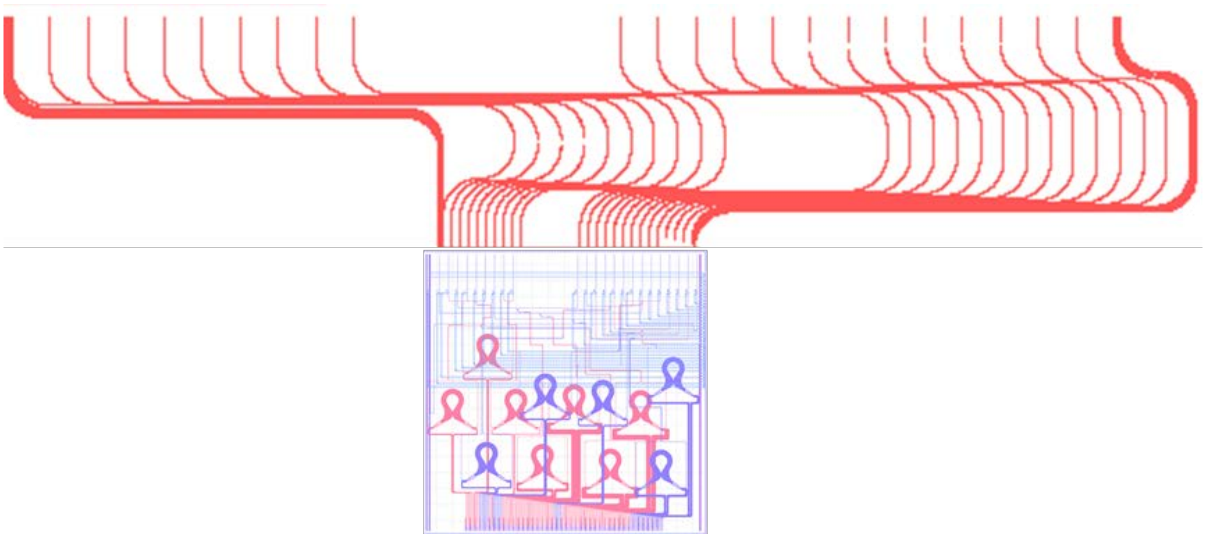


Fig 3. Layout of the high-resolution PIC.

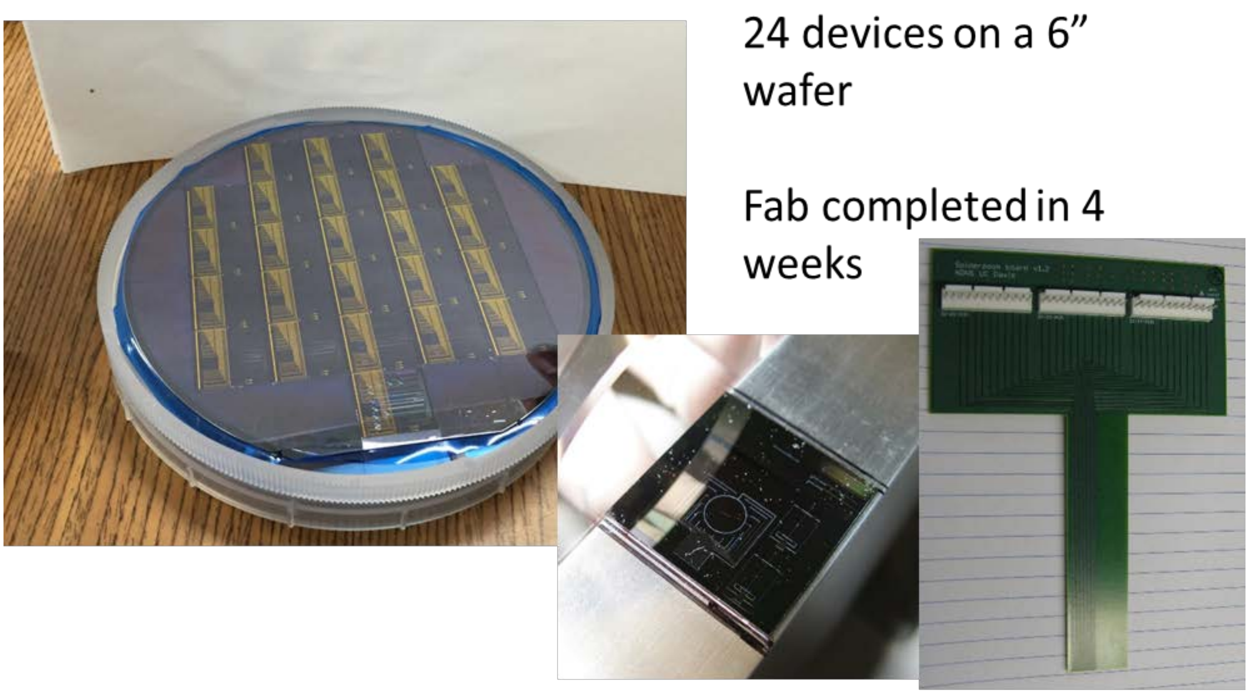
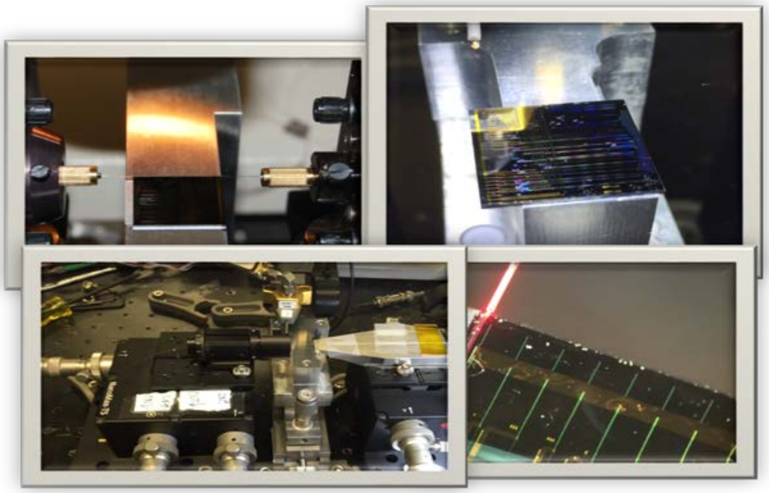


Fig 4. Pictures of low-resolution PIC wafer and devices in mounts after dicing.

4.0 SECOND-GENERATION PIC TEST RESULTS

We developed a testbed to demonstrate the SPIDER concept using a second-generation SPIDER PIC with a lenslet array. The lenslet array was aligned to couple light into the PIC from a common scene FOV using xyz stages. The beam combination output waveguides are re-imaged to a linear indium galliam arsenide (InGaAs) detector array for data collection. The printed circuit boards (PCBs) next to the PIC are used for electrical connections to the thermo-optic phase shifters that control the relative phase and to the heaters that fine-tune the spectral demux passbands. Fig 5 shows the test configuration with the low-resolution PIC under test.



- Low Resolution SPIDER PIC in test at UC Davis
- Light coupled in and out of PIC via optical fibers
- Optical throughput measurements
- Heater calibrations for phase control

Fig. 5. SPIDER PIC test configuration.

For initial testing, we use a broadband light source and launch transverse electric (TE)-mode light into the device under test from a lens fiber. At the output end, a lens fiber captures and sends the light to an OSA (optical spectrum analyzer). We scan the spectrum between 1200 nm and 1600 nm for all the inputs and all the outputs. We measure the heater resistance around 170Ω for all 24 inputs. The electrode resistance range from 10 Ω to 40 Ω, depending on the length of the electrode. From single-layer testing, we find that the energy required for 2π phase change of the heaters is around 320 mW. For any given input/output part, the total transmission is the combination of 2x2 MMI transmission and AWG transmission. We measure the 1550 nm channel from two different wafers and two dies from each wafer. Fig. 6 shows representative optical throughput measurements normalized to the straight through PIC waveguides.

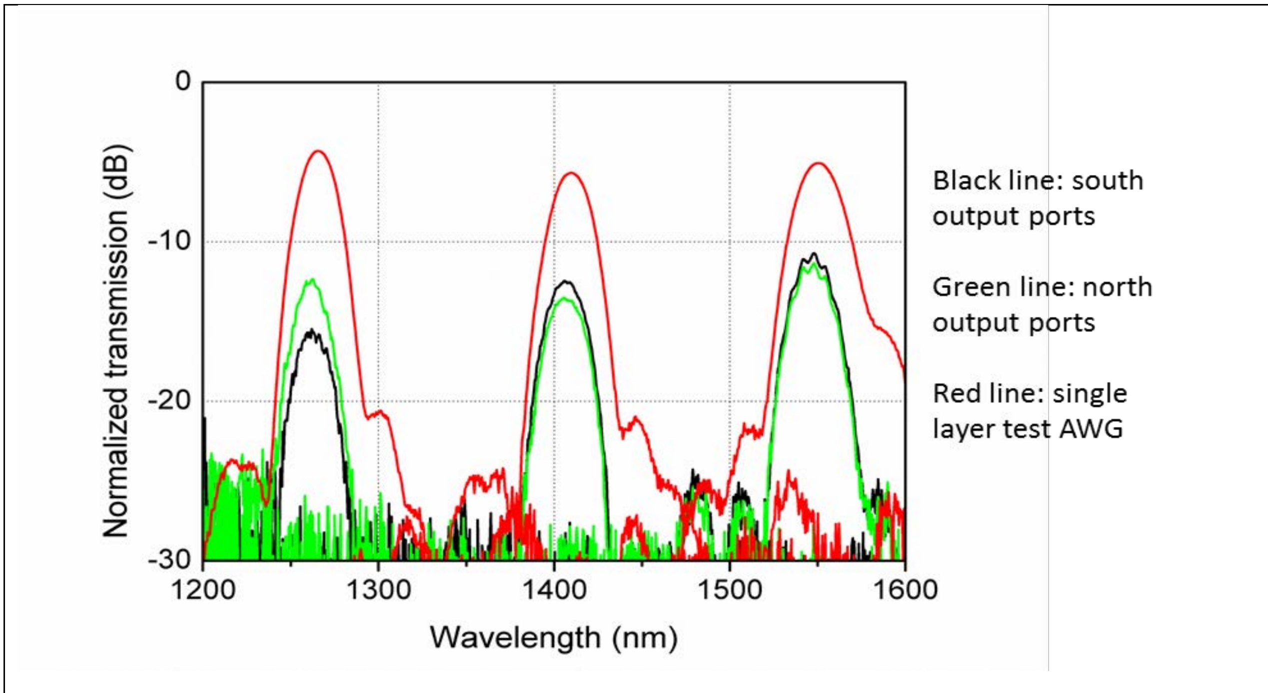


Fig. 6. Low-resolution PIC optical throughput measurements.

Fig. 7 shows fringe measurements for a representative interferometer channel.

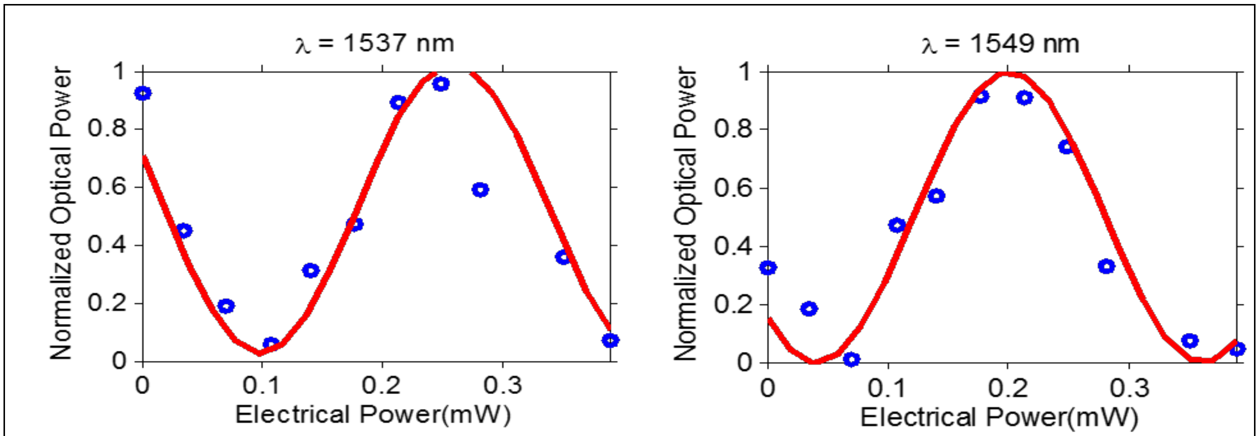


Fig. 7. Low-resolution PIC interferometer fringe measurement.

5.0 SUMMARY

Prior LM internal research and development (IRAD) and DARPA/NASA customer research and development (CRAD)-funded SPIDER risk-reduction experiments, design trades, and simulations have matured the SPIDER imager concept to Technology Readiness Level (TRL) 3. Current funding under the DARPA SPIDER Zoom program seeks to mature the underlying PIC technology for SPIDER to TRL 4. This is done by developing and fabricating a second-generation PIC that is fully traceable to the multiple layers and low-power phase modulators required for higher-dimension waveguide arrays that are needed for higher field-of-view sensors. Our project also aims to extend the SPIDER concept to add a zoom capability that provides simultaneous low-resolution, large field-of-view and steerable high-resolution, narrow field-of-view imaging modes. A proof-of-concept demo is being used to validate this capability. Data collected by this project is used to benchmark and increase the fidelity of our SPIDER image simulations and enhance our ability to predict the performance of existing and future SPIDER sensor design variations. These designs and their associated performance characteristics are then evaluated as candidates for future mission opportunities to identify specific transition paths.

6.0 REFERENCES

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7.0 ACKNOWLEDGEMENTS

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions, and/or findings contained in this material are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.